

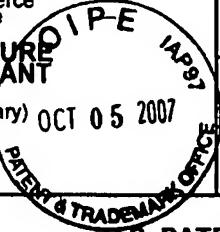
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**INFORMATION DISCLOSURE
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ATTY. DOCKET NO.

L8462.06108

SERIAL NO.

10/581,262

APPLICANT

T. SAEKI, et al.

FILING DATE

June 1, 2006

GROUP

2817
Unassigned**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER								DATE	NAME	CLASS	SUBCLASS	FILING DATE APPROPRIATE
<i>Gillig</i>		5	7	7	7	5	2	1		07/1998	Gillig Steven et al.	—	—	
2001		0	3	6	8	1	7			11/2001	Yamada Ryoichi et al.	—	—	
		6	1	0	7	8	4	3		08/2000	De Gouy Jean-Luc et al.	—	—	
		6	0	7	5	4	7	4		06/2000	Gabet Pascal et al.	—	—	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Gillig
Supplementary European Search Report dated September 4, 2007.

EXAMINER

DATE CONSIDERED

11/19/07

EXAMINER: Initial if citation is considered, draw line through citation if not in conformance and not considered.
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New PCT Nat'l Stage Application

APPLICANT

Takaharu SAEKI, et al.

FILING DATE

DATE
June 1, 2006

GROUP

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U.S. PATENT DOCUMENTS.

FOREIGN PATENT DOCUMENTS

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

PCT International Search Report dated March 22, 2006.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		APPLICANT T. SAEKI, et al.	
		FILING DATE June 1, 2006	GROUP 281 Unassigned

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H. Adachi, et al.: "High-Speed Switching Synthesizer Using Fractional N Phase Locked Loop," The Institute of Electronics, Information and Communication Engineers, Transactions C-1, Vol. J76-C-1, No. 11, November 1993, pages 445-452, with partial English translation.

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11/18/07

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